Product Features

1. SMD seam sealed clock crystal oscillator
2. Operating Temperature Range：-40~105℃
3. Temperature Stability：±0.5 ~ ± 5 ppm
4. Supply voltage range：1.68V ~ 3.63V
5. Voltage Control Function Available
6. AEC-Q100 Compliant
7. RoHS and REACH Compliant , Pb-free , Halogen-free
8. Industry Standard Package：
   3.2 x 1.5 x 1.0 mm

Application：

- Automotive GPS
- C-V2X

Test condition
Ambient temperature：25 ± 5℃
Relative humidity： 40% ~ 70%

- **Table 1 . Electrical Specifications**

Parameters	Symbol	Min.	Typ.	Max.	Units	Notes
Clipped Sinewave (CS) Type Signal Characteristics						
Nominal Frequency	F	10 ~ 52			MHz	
Frequency Tolerance	-	-	-	± 2	ppm	After 2 times reflow
Frequency Stability	ST	± 0.5 ~ ± 2.5			ppm	ST VS Temp.
		-	-	± 0.2		ST VS Output Load
		-	-	± 0.2		ST VS Supply Voltage
Operating Temperature	Topr	-40	25	105	℃	
Supply Voltage	Vdd	1.68 ~ 3.63			V	
Current Consumption	Icc	-	-	2	mA	
Output Load : CS	R Load	9	10	11	Kohm	
	C Load	9	10	11	pF	
Output Voltage Level	Vp-p	0.8	-	-	V	
Slope of Frequency Drift over Temperature	-	± 0.1 ~ ± 0.5			ppm/C	
Start-up Time	Tosc	-	-	3	ms	To 90% of Vp-p
Duty Cycle	TH/T	45	50	55	%	
Aging	-	-	-	5	ppm	10th. Year at 25℃
Phase Noise	PN	-	-	-135	dBc/Hz	@1KHz offset

Note 1：The table shows common spec. if you have special spec. requirement , please feel free to contact our salesperson.

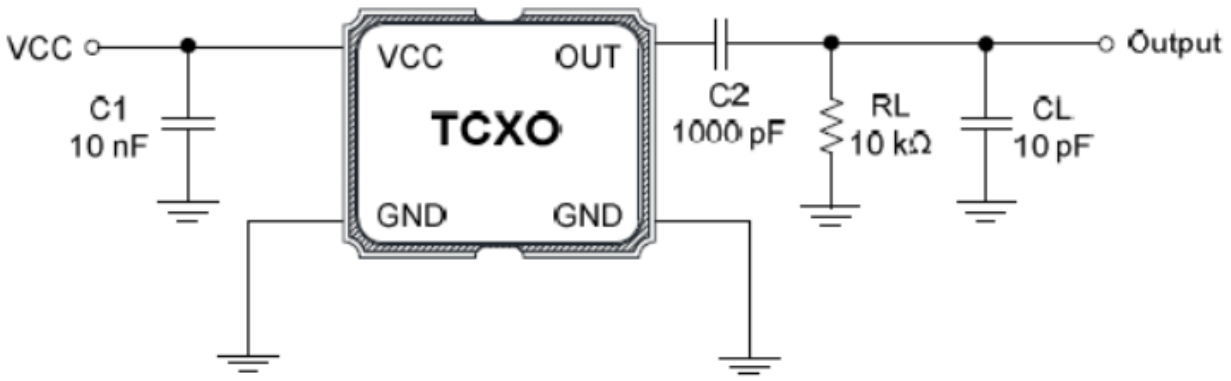
Test condition
Ambient temperature：25 ± 5℃
Relative humidity： 40% ~ 70%

- **Table 1 . Electrical Specifications (continued)**

Parameters	Symbol	Min.	Typ.	Max.	Units	Notes
CMOS Type Signal Characteristics						
Nominal Frequency	F	10 ~ 52			MHz	
Frequency Tolerance	-	-	-	± 2	ppm	After 2 times reflow
Frequency Stability	ST	± 2.5 ~ ± 5			ppm	ST VS Temp.
		-	-	± 0.2		ST VS Output Load
		-	-	± 0.2		ST VS Supply Voltage
Operating Temperature	Topr	-40	25	105	℃	
Supply Voltage	Vdd	1.68 ~ 3.63			V	
Current Consumption	Icc	-	-	5	mA	
Output Load : CMOS	CL	15			pF	
Output Voltage High	VoH	90%Vdd	-	-	V	
Output Voltage Low	VoL	-	-	10%Vdd	V	
Rise Time	Tr	-	-	5	ns	10% → 90% Vdd Level
		-	-	4	ns	20% → 80% Vdd Level
Fall Time	Tf	-	-	5	ns	90% → 10% Vdd Level
		-	-	4	ns	80% → 20% Vdd Level
Duty Cycle	TH/T	45	~	55	%	
Start-up Time	Tosc	-	-	3	ms	To 90% of Final Amplitude
Slope of Frequency Drift over Temperature	-	± 0.3 ~ ± 0.5			ppm/C	
Enable Control	-	Yes			-	Pin 1 function
Enable Voltage High	VIH	80%Vdd	-	-	V	
Disable Voltage Low	VIL	-	-	20%Vdd	V	
Aging	-	± 5			ppm	10th. Year at 25℃
Phase Noise	PN	-	-	-135	dBc/Hz	@1KHz offset

● Test Diagram

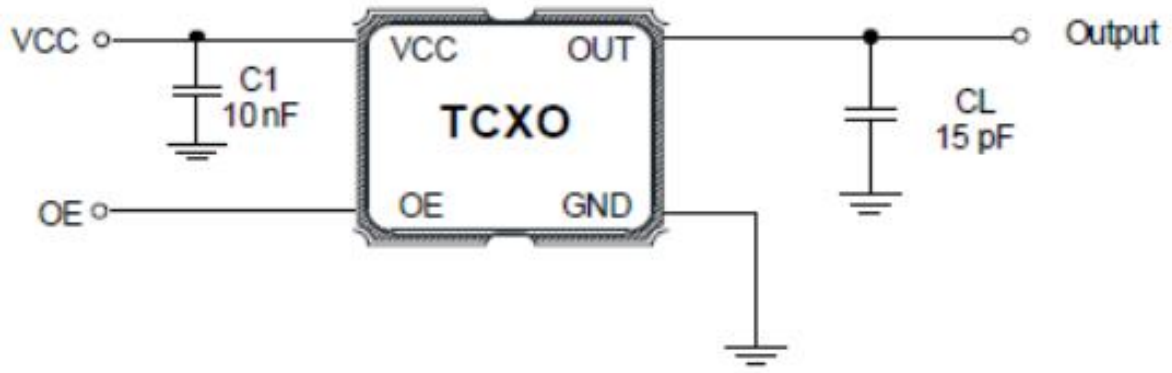
■ Clipped Sinewave Output



Name	Function
C1	AC Noise Bypass for VCC
C2	DC Block for Output
RL	Load Resistance
CL	Load Capacitance

Note : Note: Bypass capacitor (C1) and DC blocking capacitor (C2) should be placed.

■ CMOS Output

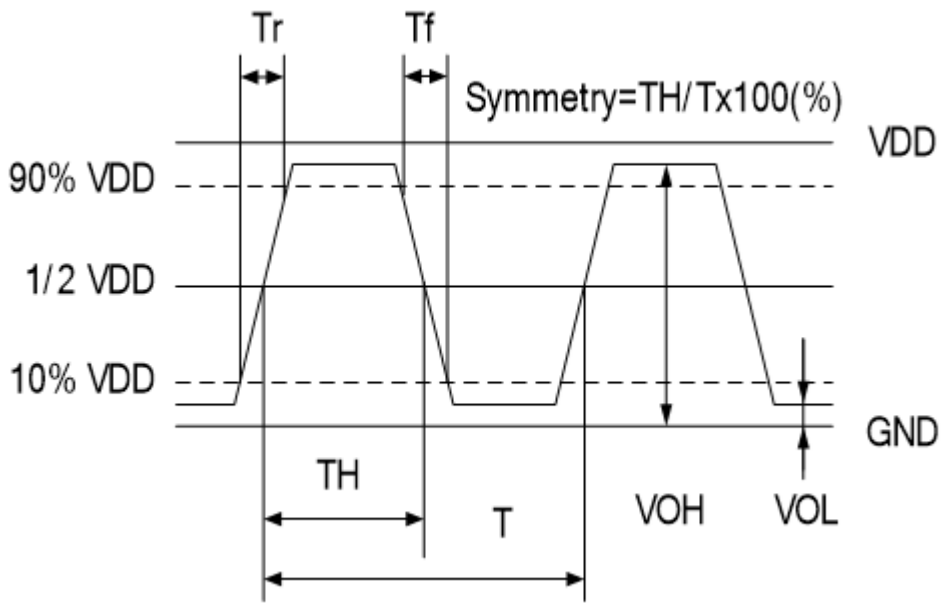


Name	Function
C1	AC Noise Bypass for VCC
CL	Load Capacitance
OE	High (or open) ↓ OSC Normal Oscillation
OE	Low ↓ OSC Stop Oscillation

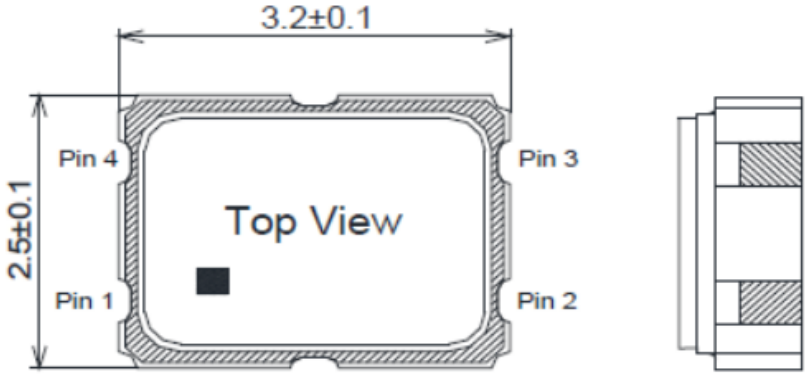
Note : TXC sets CL to 15pF for simulation IC load. Customer does not need to layout it in reality circuit.

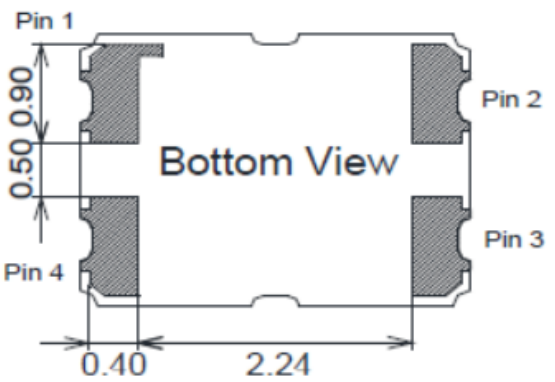
- **CMOS Output Waveform Conditions**

Waveform measurement system should have a min. bandwidth of 5 times the frequency being tested.



- **Dimensions & Footprint (Recommended)**





Unit : mm

Pin Connection

Name	Function
Pin 1	OE
Pin 2	GND
Pin 3	OUTPUT
Pin 4	VCC

Recommended Land Pattern