



Programmable Voltage Controlled Oscillator (VCXO)

Output: LV-PECL

VG7050EAN / ECN



Product Number
 EAN : X1G004541xxxx00
 ECN : X1G004561xxxx00

- Frequency range : 50 MHz to 800 MHz
(Tuning resolution: 2.2 to 2.8×10^{-9})
- Supply voltage : 2.5 V / 3.3 V
- External dimensions : EAN : $7.0 \times 5.0 \times 1.5$ mm (8 pins)
ECN : $7.0 \times 5.0 \times 1.5$ mm (10 pins)
- Absolute Pull Range : $\pm 0 \times 10^{-6}$ to $\pm 180 \times 10^{-6}$ (12 steps selectable)

Features

- EAN : User-specified one startup frequency, APR and 7-bit I²C address
- ECN : User-specified four startup frequency, APR and 7-bit I²C address
- User Programming : I²C Interface
- Low jitter PLL technology

Applications

SONET/SDH, OTN, GbE, Fibre Channel



Specifications (characteristics)

Item	Symbol	Specifications	Conditions / Remarks
Output frequency range	f _o	50 MHz to 800 MHz	It can be changed by I ² C
Supply voltage	V _{CC}	D: 2.5 V ± 0.125 V, C: 3.3 V ± 0.33 V	
Storage temperature range	T _{stg}	-55 °C to +125 °C	Store as bare product after packing
Operating temperature range	T _{use}	-40 °C to +85 °C	
Frequency tolerance *1	f _{tol}	±50 × 10 ⁻⁶	Includes frequency aging (10 years)
Current consumption	I _{CC}	90 mA Max.	OE Active, L_ECL=50 Ω
Disable current	I _{dis}	40 mA Max.	OE Inactive, Output Standby: Hi-Z mode
		70 mA Max.	OE Inactive, Output Standby: Fix mode
Absolute pull range	APR	±0 × 10 ⁻⁶ to ±180 × 10 ⁻⁶ Min.	V _c = 1.65 V ± 1.35 V (V _{CC} = 3.3 V)
		±0 × 10 ⁻⁶ to ±180 × 10 ⁻⁶ Min.	V _c = 1.25 V ± 1.00 V (V _{CC} = 2.5 V)
Control voltage tuning range	V _c	0 V to V _{CC}	
Frequency change polarity	-	Positive slope	
Symmetry	SYM	45 % to 55 %	At outputs crossing point
Output voltage	V _{OH}	V _{CC} - 1.025 V Min.	DC characteristics
	V _{OL}	V _{CC} - 1.62 V Max.	
Output load condition	L_ECL	50 Ω	Termination to V _{CC} - 2.0 V
Input voltage	V _{IH}	70 % V _{CC} Min.	EAN : OE, SDA and SCL ECN : OE, FSEL0, FSEL1, SDA and SCL
	V _{IL}	30 % V _{CC} Max.	
Rise time / Fall time	t _r / t _f	400 ps Max.	Between 20 % and 80 % of (V _{OH} - V _{OL})
Start-up time	t _{str}	10 ms Max.	Time at minimum supply voltage to be 0 s

*1 Frequency tolerance includes initial frequency tolerance, temperature variation, supply voltage change, reflow drift and 10 years aging at +25 °C.

Product name VG7050 EAN SM18xxxx C J G H P Z
 (Standard form) ① ② ③ ④ ⑤ ⑥ ⑦ ⑧ ⑨

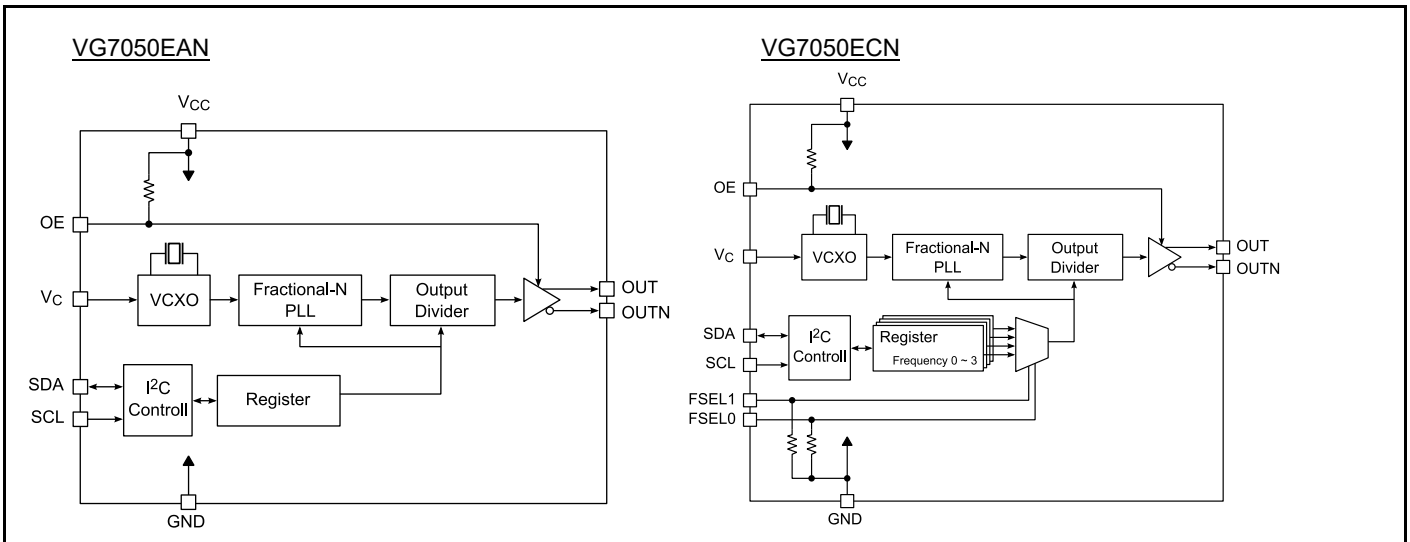
- ① Model
- ② Output (E: LV-PECL)
- ③ Parameter Designator (EAN: SM18xxxx, ECN: SM20xxxx)
- ④ Supply voltage (C: 3.3 V Typ., D: 2.5 V Typ.)
- ⑤ Frequency tolerance (J: ±50 × 10⁻⁶)
- ⑥ Operating temperature (G: -40 °C to +85 °C)
- ⑦ OE Function (H: Active High, L: Active Low)
- ⑧ Absolute Pull Range (P: Programmable)
- ⑨ Output Standby Type (F: Fix (OUT="L", OUTN="H"), Z: High-Z)

Phase Jitter

	Offset Frequency	125.00 MHz	156.25 MHz	250.00 MHz	425.00 MHz	622.08 MHz	669.33 MHz	794.73 MHz
Phase jitter*2 Typ.	12 kHz to 20 MHz	0.30 ps	0.26 ps	0.26 ps	0.25 ps	0.26 ps	0.26 ps	0.26 ps
	20 kHz to 50 MHz	0.30 ps	0.27 ps	0.27 ps	0.26 ps	0.27 ps	0.27 ps	0.27 ps
	50 kHz to 80 MHz	0.29 ps	0.27 ps	0.27 ps	0.26 ps	0.27 ps	0.27 ps	0.27 ps

*2 In order to achieve optimum jitter performance, it is recommended that the capacitor (0.1 μF + 10 μF) between V_{CC} and GND pin should be placed as close to the V_{CC} pin as possible.

Block diagram

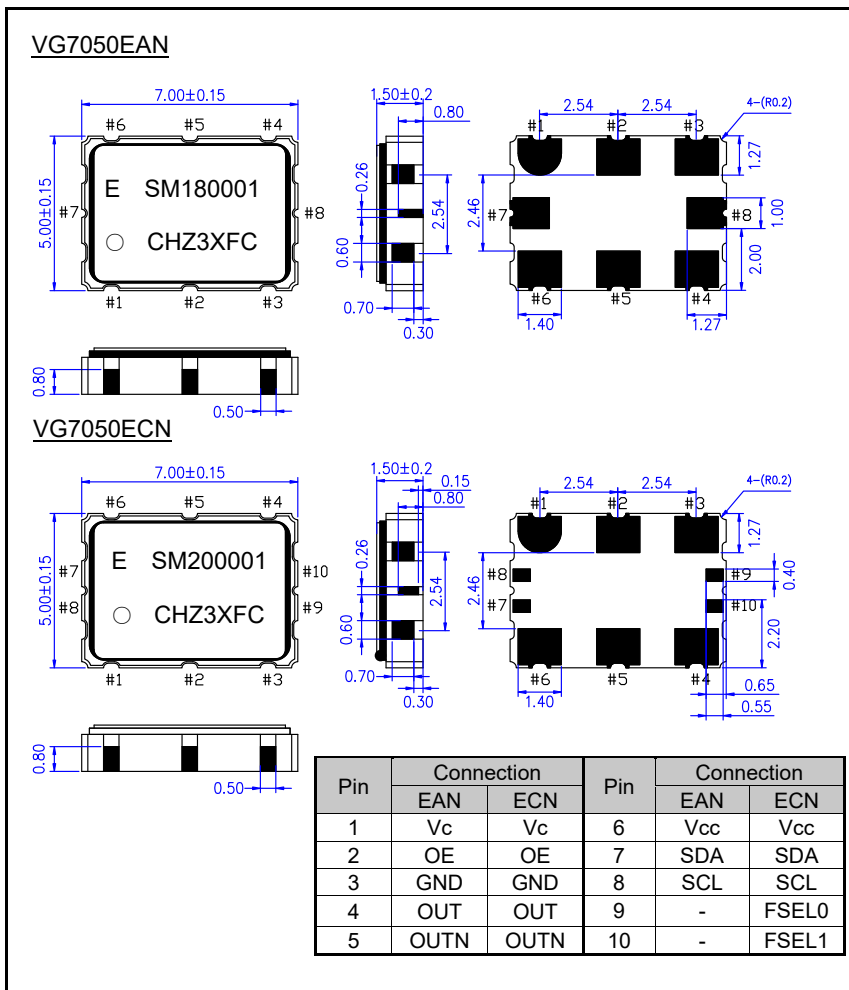


OE Function / OE Standby Type

OE Function	OE Standby Type	Output Enable		
		OE pin	Output Disable	
H: High Active	Z: High-Z	"H" or "OPEN"	"L"	High Impedance
L: Low Active		"L" or "OPEN"	"H"	
H: High Active	F: Fix	"H" or "OPEN"	"L"	OUT = "L", OUTN = "H"
L: Low Active		"L" or "OPEN"	"H"	

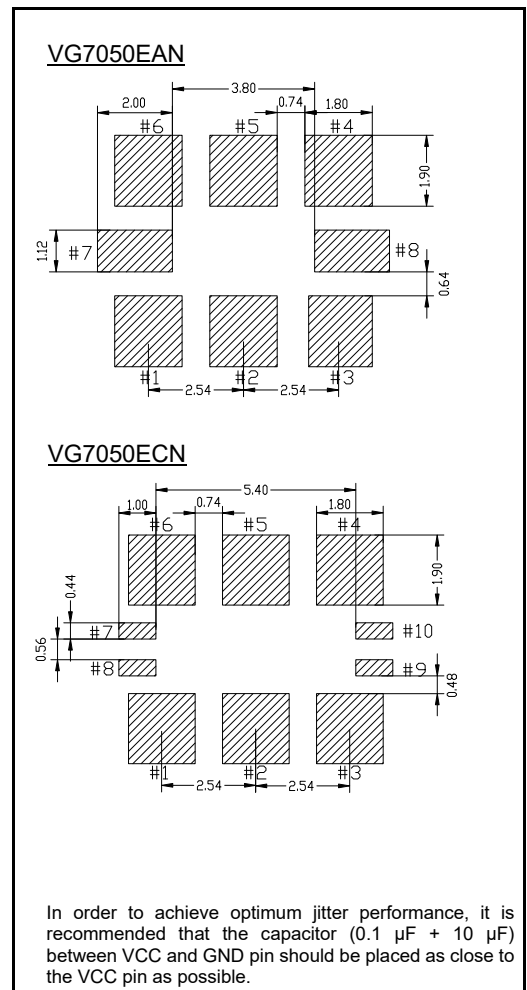
External dimensions

(Unit: mm)



Footprint (Recommended)

(Unit: mm)



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