Features

- AEC-Q100 Grade 1 temperature range
- 44 fixed frequencies between 4 MHz and 125 MHz
- Supply voltage of 1.5 V, 1.8 V, 2.5 V and 3.3 V (Contact SiTime for 1.2 V)
- Low power consumption of 2.5 mA typical at 1.8 V
- LVCMOS compatible output
- 1 µA standby current
- 450 fs RMS phase jitter
- Industry-standard packages: 2.0 x 1.6, 2.5 x 2.0, 3.2 x 2.5 mm (Contact SiTime for 1.6 x 1.2 mm)
- RoHS and REACH compliant, Lead-free, Halogen-free and Antimony-free

Applications

- Automotive Camera and Sensors, Smart Mirrors
- Advanced Driver Assistance Systems
- Automotive Infotainment Systems
- In-vehicle networking and SerDes
- Industrial sensors

Related products for **automotive applications**

For aerospace and defense applications SiTime recommends using only **Endura™ ruggedized products**

Order samples

Electrical Specifications

Table 1. Electrical Characteristics

All Min and Max limits are specified over temperature for all supply voltages with 15 pF output load unless otherwise stated. Typical values are specified at 25°C and at the nominal value of the highest voltage option for that parameter.

Parameters	Symbol	Min.	Typ.	Max.	Unit	Condition
Frequency Range						
Fixed Frequency Options	f	5, 10, 20, 25, 31.25, 33.333333, 50, 62.5, 78.125, 100, 125			MHz	SiT1625A
		4, 4.096, 6, 8, 8.192, 9, 12, 16, 18, 18.432, 19.2, 24, 24.576, 30.72, 32, 32.768, 36, 38.4, 48, 61.44, 64, 72, 76.8, 96, 122.88				SiT1625B
		7, 13, 21, 27, 39, 63, 91, 117				SiT1625C
Frequency Stability and Aging						
Frequency Stability	F_stab	-50	–	+50	ppm	Inclusive of Initial tolerance at 25°C, 1st year aging at 25°C, and variations over operating temperature -40°C to 125°C, rated power supply voltage and load (15 pF ±10%)
		-30	–	+30		Supported for -40°C to 105°C
		-25	–	+25		Supported for -40°C to 85°C
Operating Temperature Range						
Operating Temperature Range	T_use	-40	–	+125	°C	AEC-Q100 Grade 1
		-40	–	+105	°C	AEC-Q100 Grade 2
		-40	–	+85	°C	AEC-Q100 Grade 3
Supply Voltage						
Supply Voltage	Vdd_1.5	1.35	1.5	1.65	V	Contact SiTime for 1.2 V and 5 V options (±5%)
	Vdd_1.8	1.62	1.8	1.98		
	Vdd_2.5	2.25	2.5	2.75		
	Vdd_3.3	2.97	3.3	3.63		
	Vdd_YY	1.62	–	3.63		

Table 1. Electrical Characteristics (continued)

Parameters	Symbol	Min.	Typ.	Max.	Unit	Condition
Current Consumption						
Current Consumption	Idd	–	2.5	–	mA	f = 27 MHz, no load, Vdd_1.5
		–	2.5	–	mA	f = 27 MHz, no load, Vdd_1.8
		–	2.6	–	mA	f = 27 MHz, no load, Vdd_2.5
		–	2.7	–	mA	f = 27 MHz, no load, Vdd_3.3
		–	2.7	–	mA	f = 27 MHz, no load, Vdd_YY, tested at Vdd_3.3
Standby Current	I_std	–	0.15	–	µA	Up to 125°C, $\overline{ST}$ = 0
		–	0.15	–		Up to 105°C, $\overline{ST}$ = 0
Mid-Standby Current	I_midstd	–	0.33	–	mA	Up to 125°C, $\overline{MS}$ = 0
		–	0.33	–		Up to 105°C, $\overline{MS}$ = 0
LVCMOS Output Characteristics						
Duty Cycle	DC	45	–	55	%	All Vdd levels
Rise/Fall Time	Tr, Tf	–	–	2.3	ns	Vdd = 1.62 V – 3.63 V, 20% - 80%, 15 pF Load, f = 27 MHz
		–	–	2.5	ns	Vdd = 1.35 V – 1.65 V, 20% - 80%, 15 pF Load, f = 27 MHz
Output High Voltage	VOH	90%	–	–	Vdd	IOH = -4 mA (Vdd = 3.0 V or 3.3 V) IOH = -3 mA (Vdd = 2.8 V and Vdd = 2.5 V) IOH = -2 mA (Vdd = 1.8 V) IOH = -1.5 mA (Vdd = 1.5 V)
Output Low Voltage	VOL	–	–	10%	Vdd	IOL = 4 mA (Vdd = 3.0 V or 3.3 V) IOL = 3 mA (Vdd = 2.8 V and Vdd = 2.5 V) IOL = 2 mA (Vdd = 1.8 V) IOL = 1.5 mA (Vdd = 1.5 V)
Input Characteristics						
Input High Voltage	VIH	70%	–	–	Vdd	Pin 1, OE or $\overline{ST}$ or $\overline{MS}$
Input Low Voltage	VIL	–	–	30%	Vdd	Pin 1, OE or $\overline{ST}$ or $\overline{MS}$
Input Pull-down Impedance	Z_in	2	–	–	MΩ	Pin 1, OE or $\overline{ST}$ or $\overline{MS}$ or NC
Startup and Resume Timing						
Startup Time	T_start	–	0.7	1	ms	Measured from the time Vdd reaches its rated minimum value
Enable/Disable Time	T_oe	–	–	210	ns	f = 27 MHz. For other frequencies, T_oe = 100 ns + 3*cycles
Resume Time (Standby)	T_resume	–	0.7	1	ms	
Resume Time (Mid-Standby)		–	0.1	–	ms	
Jitter and Phase Noise						
RMS Period Jitter[1]	T_jitt	–	1	–	ps	f = 27 MHz, measured based on 10k cycles
RMS Phase Jitter (random)[2]	T_phj_fc_2	–	0.45	–	ps	f = 27 MHz, 12 kHz – 20 MHz integration bandwidth, phase noise measured 12 kHz – 10 MHz and extended flat above 10 MHz
	T_phj_5	–	0.33	–	ps	f = 27 MHz, 12 kHz – 5 MHz integration bandwidth, phase noise measured 12 kHz – 5 MHz
	T_phj_fc48	–	0.42	–	ps	f = 48 MHz, 12 kHz – 20 MHz integration bandwidth, phase noise measured 12 kHz – 20 MHz
Phase Noise	PN	–	-145	–	dBc/Hz	f = 27 MHz, f_offset = 100 kHz
Spurious Phase Noise	T_spn	–	-85	–	dBc	f = 27 MHz, 1.8 V, 12 kHz – 5 MHz offset frequency range
Power Supply-Induced Jitter Sensitivity	PSJS	–	0.4	–	ps/mV	50 mV peak-peak on Vdd = 3.3 V

Note:

1. Appropriate when driving digital logic for use in setup and hold time equations.
2. Appropriate when driving phase locked loops in high-speed SerDes applications.

Table 2. Absolute Maximum Limits

Operation outside the absolute maximum ratings may cause permanent damage to the part.
Performance of the IC is only guaranteed within the operational specifications, not at absolute maximum ratings.

Parameter	Min.	Max.	Unit
Storage Temperature	-65	150	°C
Supply Voltage (Vdd)	-0.5	4	V
Electrostatic Discharge (HBM)	–	2000	V
Electrostatic Discharge (CDM)	–	750	V
Soldering Temperature (follow standard Pb free soldering guidelines)[3]	–	260	°C
Junction Temperature[4]	–	150	°C

Note:

3. Please refer to SiTime Manufacturing Notes.
4. Exceeding this temperature for extended period of time may damage the device.

Table 3. Thermal Considerations[5]

Package	θ_{JA} (°C/W)	θ_{JB} (°C/W)	θ_{JC} (°C/W)	Ψ_{JT} (°C/W)
3225	208	76	134	15.7
2520	187	78	133	16.4
2016	190	75	167	14.9
1612	TBD	TBD	TBD	TBD

Note:

5. θ_{JA}, Ψ_{JT}, θ_{JB} and θ_{JC} are provided according to JEDEC standards 51-2A, 51-7, 51-8, and 51-12.01 with a 25°C ambient and 36.3 mW power consumption. The conduction thermal resistances θ_{JB} and θ_{JC} are obtained with the assumption that all heat flows from the junction to a heat sink through either the solder pads (θ_{JB}) or the top of the package (θ_{JC}). The values of θ_{JA} and Ψ_{JT} are strongly application dependent, and we report values based on the JEDEC thermal environment of 2s2p board and still air. θ_{JA} is the thermal resistance to ambient on a JEDEC PCB - it is a conservative estimate, since the JEDEC board does not have vias to PCB planes in the vicinity of the package. Ψ_{JT} can be used to estimate the junction temperature from accurate measurements of the temperature at the top of the package if the thermal environment is similar to the JEDEC environment.

Table 4. Maximum Operating Junction Temperature[6]

Max Operating Temperature (ambient)	Maximum Operating Junction Temperature
85°C	95°C
105°C	115°C
125°C	135°C

Note:

6. Datasheet specifications are not guaranteed if junction temperature exceeds the maximum operating junction temperature.

Table 5. Environmental Compliance

Parameter	Condition/Test Method
Mechanical Shock	**MIL-STD-883F, Method 2002**
Mechanical Vibration	**MIL-STD-883F, Method 2007**
Temperature Cycle	**JESD22, Method A104**
Solderability	**MIL-STD-883F, Method 2003**
Moisture Sensitivity Level	**MSL1 @ 260°C**

Pin Description

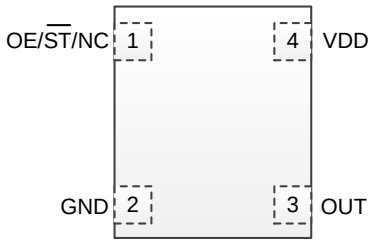


Figure 1. Pin Assignments (Top View)

Table 6. Pin Description

Pin	Symbol		Function
1	OE/ $\overline{ST}$ /$\overline{MS}$ /NC	Output Enable (OE)	H[7]: specified frequency output L: output is high impedance. Only output driver is disabled
		Standby ($\overline{ST}$)	H[7]: specified frequency output L: output is low (weak pull down). Device goes to sleep mode
		Mid-Standby ($\overline{MS}$)	H[7]: specified frequency output L: output is low (weak pull down). Device goes to mid-standby mode
		No Connect (NC)	Any voltage between GND and Vdd or Open[8]. Specified frequency output. Pin 1 has no function.
2	GND	Power	Electrical ground[8]
3	OUT	Output	Oscillator output
4	VDD	Power	Power supply voltage[8]

Notes:

7. In OE or $\overline{MS}$ or $\overline{ST}$ mode, a pull-up resistor of 10 KΩ or less is recommended if pin 1 is not externally driven. If pin 1 needs to be left floating, use the NC option.
8. A capacitor of value 0.1 µF between VDD and GND is required.

Test Circuit and Waveform

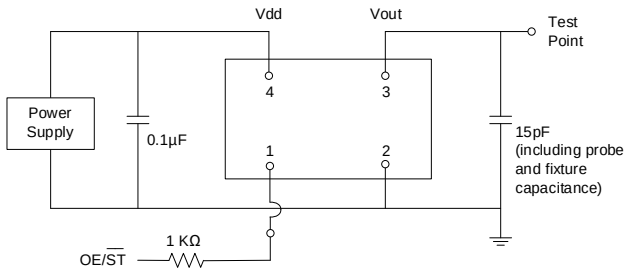


Figure 2. Test Circuit[9]

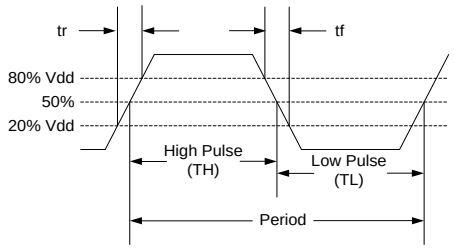


Figure 3. Waveform[9]

Note:

9. Duty Cycle is computed as Duty Cycle = TH/Period.

Timing Diagrams

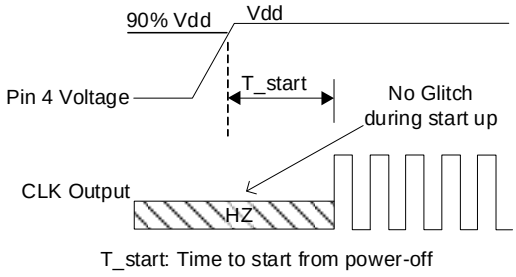


Figure 4. Startup Timing (OE/$\overline{ST}$ Mode)[10]

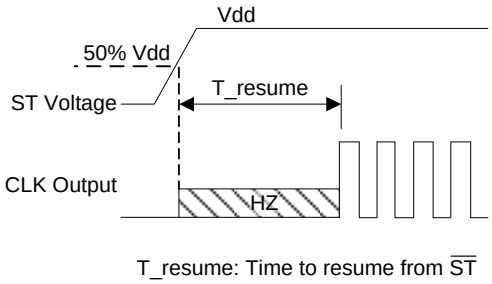


Figure 5. Standby Resume Timing ($\overline{ST}$ Mode Only)[10]

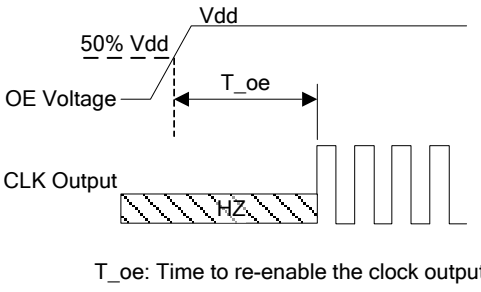


Figure 6. OE Enable Timing (OE Mode Only)

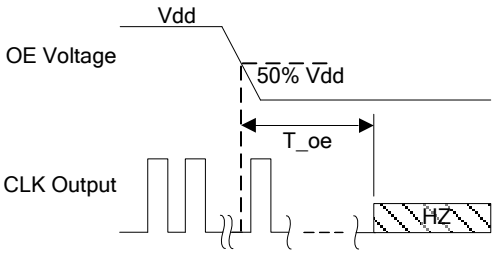


Figure 7. OE Disable Timing (OE Mode Only)

Note:

10. SiT1625 has “no runt” pulses and “no glitch” output during startup or resume.

Programmable Drive Strength

The SiT1625 includes a programmable drive strength feature to provide a simple, flexible tool to optimize the clock rise/fall time for specific applications. Benefits from the programmable drive strength feature are:

- Improves system radiated electromagnetic interference (EMI) by slowing down the clock rise/fall time.
- Improves the downstream clock receiver's (RX) jitter by decreasing (speeding up) the clock rise/fall time.
- Ability to drive large capacitive loads while maintaining full swing with sharp edge rates.

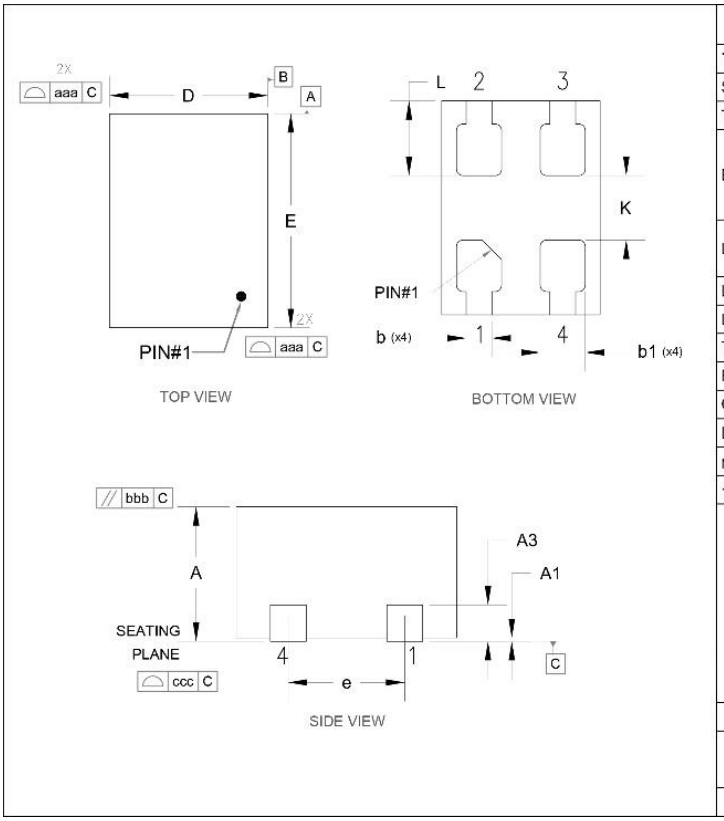
Table 1 reflects the default drive strength which is optimized for fastest rise/fall times.

For more detailed information about rise/fall time control and drive strength selection, contact SiTime.

Dimensions and Patterns

Package Size – Dimensions (Unit: mm)[11]

1.6 x 1.2 x 0.75 mm



		SYMBOL	MIN	NOM	MAX
TOTAL THICKNESS		A	0.700	0.750	0.800
STAND OFF LEAD		A1	0.000	0.020	0.050
THICKNESS		A3		0.203 REF	
BODY SIZE	X	D	1.180	1.230	1.280
	Y	E	1.610	1.660	1.710
LEAD WIDTH		b	0.150	0.200	0.250
		b1	0.300	0.350	0.400
LEAD LENGTH		L	0.480	0.580	0.680
LEAD PITCH PACKAGE		e		0.650 BSC	
TOLERNCE MOLD		aaa		0.150	
FLATNESS		bbb		0.100	
COPLANARITY		ccc		0.080	
LEAD DISTANCE		K		0.50 REF	

NOTE

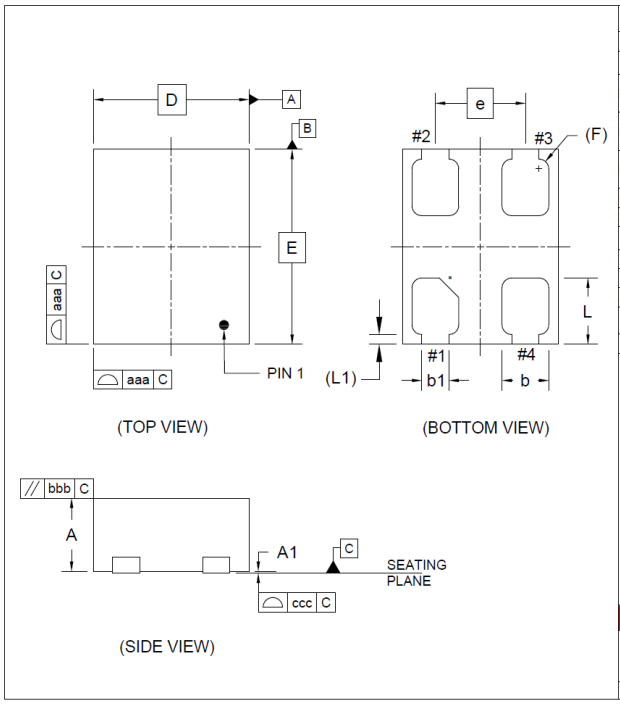
1. ALL DIMENSIONS IN MM

SiTime

PKG INFO		DRAWING NO.
4L PQFN 1.230x1.660x0.750 mm		POD-096-PQFN-004-G01216
		REV
DATE	13-Apr-2023	A00

Package Size – Dimensions (Unit: mm)[11]

2.0 x 1.6 x 0.75 mm



		SYMBOL	MIN	NOM	MAX
PACKAGE THICKNESS		A	0.700	0.750	0.800
STAND OFF		A1	0.000	0.020	0.050
BODY SIZE	X	D		1.600 BSC	
	Y	E		2.000 BSC	
LEAD WIDTH		b	0.430	0.480	0.530
		b1	0.230	0.280	0.330
LEAD LENGTH		L	0.580	0.680	0.780
		L1		0.100 REF	
LEAD PITCH		e		0.930 BSC	
RADIUS		F		0.100 REF	
PACKAGE TOLERANCE		aaa		0.050	
MOLD FLATNESS		bbb		0.100	
COPLANARITY		ccc		0.080	

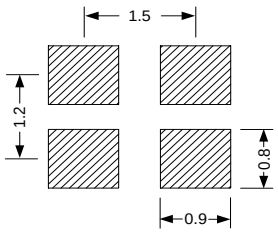
NOTES

1. Dimensioning and tolerance conform to ASME Y14.5-2009
2. All dimensions are in millimeters.

SiTime

TITLE		DWG NO.	
4L PQFN 1.60x2.00x0.75 mm		POD-PQFN-004-X01620-026	
		REV.	SHEET
DATE	01-APR-2019	A02	1 OF 2

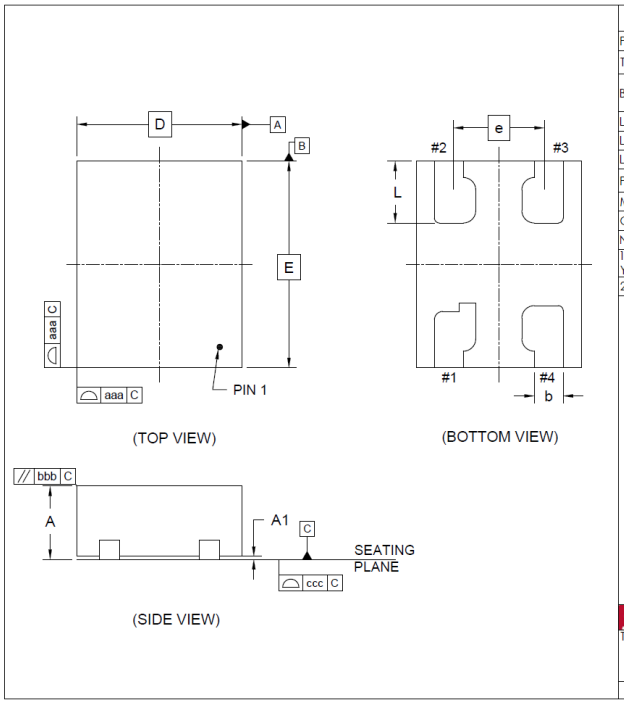
Recommended Land Pattern (Unit: mm)[12]



Dimensions and Patterns (continued)

Package Size – Dimensions (Unit: mm)[11]	Recommended Land Pattern (Unit: mm)[12]

2.5 x 2.0 x 0.75 mm

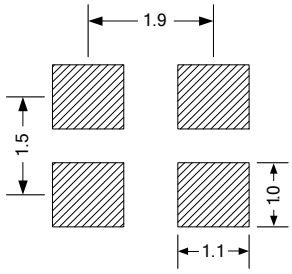


		SYMBOL	MIN	NOM	MAX
PACKAGE THICKNESS		A	0.700	0.750	0.800
THICKNESS		A1	0.000	0.020	0.050
BODY SIZE	X	D		2.000 BSC	
	Y	E		2.500 BSC	
LEAD WIDTH		b	0.300	0.350	0.400
LEAD LENGTH		L	0.650	0.750	0.850
LEAD PITCH		e		1.250 BSC	
PACKAGE TOLERANCE		aaa		0.050	
MOLD FLATNESS		bbb		0.100	
COPLANARITY		ccc		0.080	

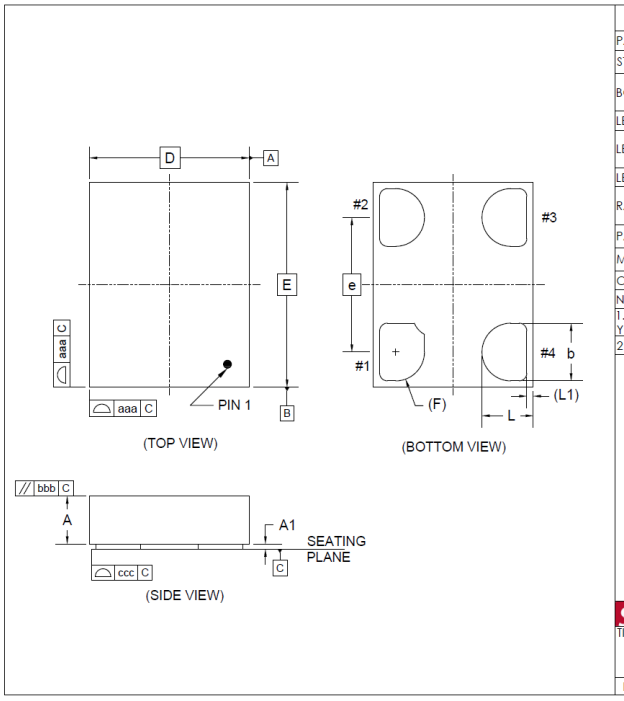
NOTES
1. Dimensioning and tolerance conform to ASME Y14.5-2009
2. All dimensions are in millimeters.

SiTime

TITLE	DWG NO.
4L PQFN	POD-PQFN-004-X02025-010
2.00x2.50x0.75 mm	REV. A02 / SHEET 1 OF 2
DATE 01-APR-2019	



3.2 x 2.5 x 0.75 mm

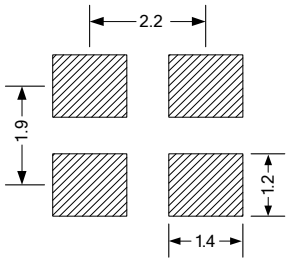


		SYMBOL	MIN	NOM	MAX
PACKAGE THICKNESS		A	0.700	0.750	0.800
STAND OFF		A1	0.000	0.020	0.050
BODY SIZE	X	D		2.500 BSC	
	Y	E		3.200 BSC	
LEAD WIDTH		b	0.800	0.900	1.000
LEAD LENGTH		L	0.700	0.800	0.900
		L1		0.100 REF	
LEAD PITCH		e		2.100 BSC	
RADIUS		F		0.450 REF	
		F1		0.120 REF	
PACKAGE TOLERANCE		aaa		0.050	
MOLD FLATNESS		bbb		0.100	
COPLANARITY		ccc		0.080	

NOTES
1. Dimensioning and tolerance conform to ASME Y14.5-2009
2. All dimensions are in millimeters.

SiTime

TITLE	DWG NO.
4L PQFN	POD-PQFN-004-X03225-002
3.20x2.50x0.75 mm	REV. A04 / SHEET 1 OF 2
DATE 01-APR-2019	

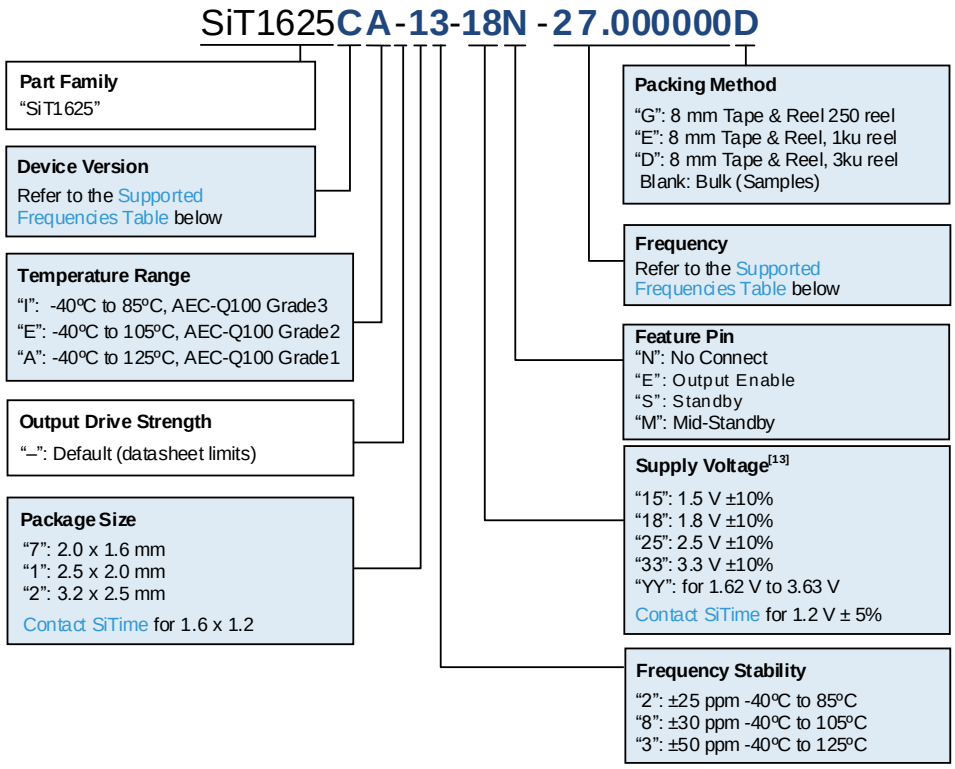


Notes:

11. Top marking: Y denotes manufacturing origin and XXXX denotes manufacturing lot number. The value of "Y" will depend on the assembly location of the device.
12. A capacitor of value 0.1 pF or higher between VDD and GND is required.

Ordering Information

The part number guide illustrated below is for reference only, in which boxes identify order codes having more than one option. To customize and build an exact part number, use the SiTime Part Number Generator. To validate the part number, use the SiTime Part Number Decoder.



Note:

13. The voltage portion of the SiT1625 part number consists of a two-digit number that denotes the specific supply voltage of the device. Alternatively, "YY" can be used to indicate the entire operating voltage range from 1.62 V to 3.63 V.

Table 7. Part Number and Supported Frequencies[14,15]

Frequency Range (MHz)							
SiT1625A		SiT1625B				SiT1625C	
5.000000	50.000000	4.000000	16.000000	32.000000	72.000000	7.000000	39.000000
10.000000	62.500000	4.096000	18.000000	32.768000	76.800000	13.000000	63.000000
20.000000	78.125000	6.000000	18.432000	36.000000	96.000000	21.000000	91.000000
25.000000	100.000000	8.000000	19.20000	38.400000	122.880000	27.000000	117.000000
31.250000	125.000000	8.192000	24.000000	48.000000	-	-	-
33.333333	-	9.000000	24.576000	61.440000	-	-	-
-	-	12.000000	30.720000	64.000000	-	-	-

Notes:

14. Any frequency the table above is supported with 6 decimal places of accuracy.
15. Please contact SiTime for frequencies that are not listed in the tables above.

Table 8. Ordering Codes for Supported Tape & Reel Packing Method

Device Size (mm^2)	8 mm T&R (3ku)	8 mm T&R (1ku)	8 mm T&R (250u)
1.6 x 1.2	D	E	G
2.0 x 1.6	D	E	G
2.5 x 2.0	D	E	G
3.2 x 2.5	D	E	G

Instant Samples with Time Machine and Field Programmable Oscillator

SiTime supports a field programmable version of the SiT1625 for fast prototyping and real time customization of features. The field programmable devices (FP devices) are available for all standard SiT1625 package sizes and can be configured to one's exact specification using the Time Machine II.

For more information regarding SiTime's field programmable solutions, see Time Machine II and Field Programmable devices.

SiT1625 is typically factory-programmed per customer ordering codes for volume delivery.

Additional Information

Table 9. Additional Information

Document	Description	Download Link
Time Machine II	Asterix programmer for engineering samples	https://www.sitime.com/time-machine-oscillator-and-active-resonator-programmer
Field Programmable Oscillators	Devices that can be programmable in the field by Time Machine II	https://www.sitime.com/support/resource-library/datasheets/field-programmable-oscillators-and-active-resonators-datasheet
Manufacturing Notes	Tape & Reel dimension, reflow profile and other manufacturing related info	https://www.sitime.com/sites/default/files/gated/Manufacturing-Notes-for-SiTime-Products.pdf
Qualification Reports	RoHS report, reliability reports, composition reports	http://www.sitime.com/support/quality-and-reliability
Performance Reports	Additional performance data such as phase noise, current consumption and jitter for selected frequencies	http://www.sitime.com/support/performance-measurement-report
Termination Techniques	Termination design recommendations	http://www.sitime.com/support/application-notes
Layout Techniques	Layout recommendations	http://www.sitime.com/support/application-notes

Revision History

Table 10. Revision History

Version	Release Date	Change Summary
0.1	3-Feb-2022	Initial release
0.22	15-Aug-2022	General Updates
0.23	21-Sep-2022	Additional updates on typos
0.24	30-Oct-2022	Formatting updates
0.25	6-Nov-2022	Adjusted frequency and package options Updated jitter and phase noise specifications
0.26	11-Feb-2023	Added clarifying notes to jitter and phase noise specifications
0.5	11-Feb-2023	Updated Features and Applications, Electrical Characteristics, Pin Descriptions, Ordering Information
0.51	22-Feb-2023	Updated Electrical Characteristics
0.52	19-Apr-2023	Added 1612 package option
0.6	27-Jul-2023	Expanded Supported Frequencies, Updated Table 1 specs, Added Programmable Drive Strength Section, Reorganized Sections, Typo corrections, Updated Ordering Information, Updated ESD spec
0.7	23-Jan-2024	Electrical Characteristics, Features, Pinout Updated

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