SiT1811

Ultra Low Power, Low-Jitter, 32.768 kHz Oscillator

Features

- Fout = 32.768 kHz
- Frequency stability of ±20 ppm
- Small Oscillator Footprint: 1.32 mm^2
  - 1.2 x 1.1 mm QFN
- Ultra-low power: 510 nA typical
- Supply voltage: 1.35 V to 1.98 V
- Operating temperature range: from -10°C to +85°C
- Pb-free, RoHS and REACH compliant

Applications

- Wearables and Hearables
- Health and wellness monitors
- Gaming and remote controllers
- AR/VR headsets

Block Diagram

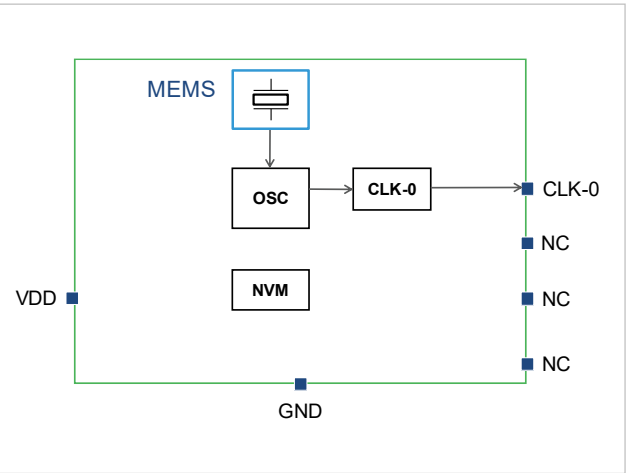


Figure 1. Block Diagram

1.2 x 1.1 mm Package Pinout

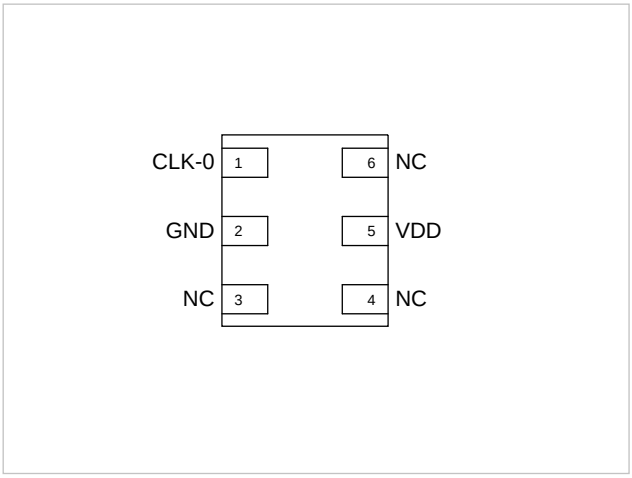
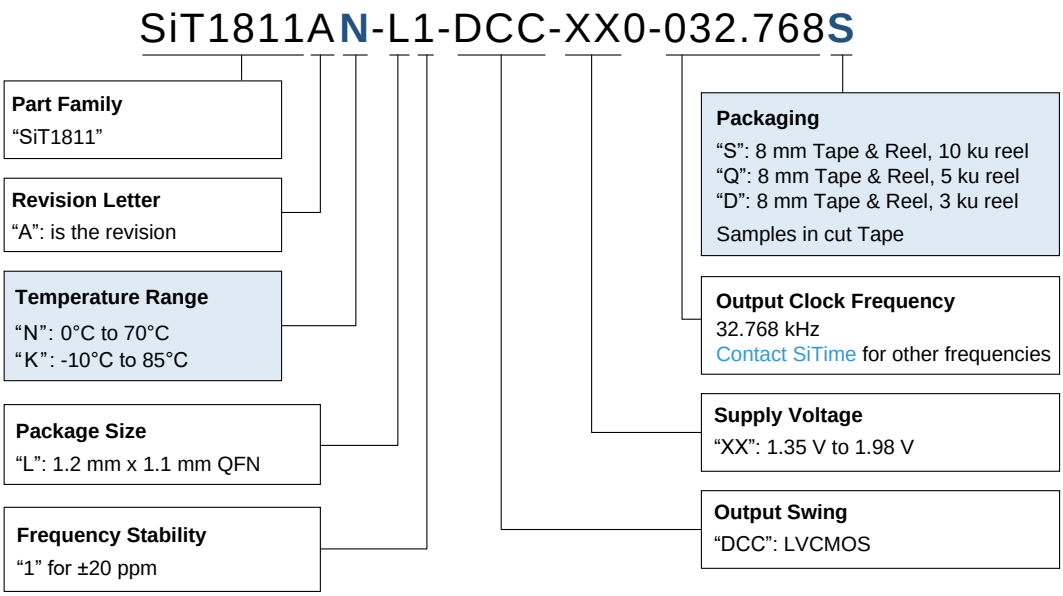


Figure 2. Pin Assignments (Top view)

(Refer to Table 4 for Pin Descriptions)

Ordering Information



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Electrical Characteristics

Table 1. Electrical Characteristics

Conditions: Min/Max limits are over temperature, V_{DD} = 1.35 - 1.98 V, unless otherwise stated.
Typical are at 25°C and V_{DD} = 1.8 V.

Parameter	Symbol	Min.	Typ.	Max.	Unit	Condition
Frequency and Stability						
Output Frequency	F_{OUT}		32.768		kHz	32.768 kHz Output. Contact SiTime for other frequencies
Initial Frequency Tolerance	F_tol	-20	–	+20	ppm	Includes 2x reflow, at 25°C
Frequency Stability[1],[2]	F_stab	-20	–	20	ppm	Over temperature, V_{DD}, aging @25°C, and 20% load variation. Temperature Ordering Codes N and K only.
Jitter Performance						
Integrated Phase Jitter	IPJ	–	3	9	ns_{RMS}	F_{OUT} = 32 kHz. Integration bandwidth = 100 Hz to 16 kHz. Inclusive of 50 mV peak-to-peak sinusoidal noise on V_{DD}. Noise frequency 100 Hz to 20 MHz.
RMS Period Jitter	PJ	–	2.5	8	ns_{RMS}	Cycles = 10,000, f = 32.768 kHz. Per JEDEC standard 65B
Supply Voltage and Current Consumption						
Operating Supply Voltage	V_{DD}	1.35	–	1.98	V	Ordering Code: XX. Contact SiTime for 1.2V operation.
No Load Supply Current	I_{DD}	–	510	635	nA	Fout = 32.768 kHz, VDD = 1.8 V; Operating Range: -10°C to 85°C
Start-up Time at Power-up	t_start	–	–	115	ms	Measured when supply reaches 90% of final V_{DD} to the first output pulse.
Output Characteristics						
Output Rise/Fall Time	t_R, t_F		20	40	ns	15 pF load, 20% to 80% of V_{DD} for LVCMOS. 20% to 80% of V_{OH} for Reduced Swing outputs. Factory Programmable Rise/Fall times. Contact SiTime for details.
Output Clock Duty Cycle	DC	45	–	55	%	
LVCMOS Output						
Output Voltage High	VOH	90%	–		V_{DD}	I_{OH} = -1 µA Contact SiTime for reduced swing options
Output Voltage Low	VOL	–	–	10%	V_{DD}	I_{OL} = 1 µA Contact SiTime for reduced swing options
Operating Temperature Range						
Operating Temperature Range	Op_Temp	0	–	+70	°C	Ordering Code (N); can support ±20 ppm stability
		-10	–	+85	°C	Ordering Code (K); can support ±20 ppm stability

Notes:

1. Tested with Agilent 53132A frequency counter. Measured with ≥100 ms gate time for accurate frequency measurement.
2. Total stability over temperature includes Initial Frequency Tolerance and Frequency Stability.

Table 2. Absolute Maximum Ratings

Attempted operation outside the absolute maximum ratings may cause permanent damage to the part.
Actual performance of the IC is only guaranteed within the operational specifications, not at absolute maximum ratings.

Parameters	Test Conditions	Value	Unit
Continuous Power Supply Voltage Range (V_{DD})		-0.5 to 2.2	V
Human Body Model (HBM) ESD Protection	JESD22-A114	2000	V
Charge-Device Model (CDM) ESD Protection	JESD22-C101	500	V
Latch-up Tolerance	JESD78 Compliant		
Mechanical Shock Resistance	Mil 883, Method 2002	20,000	*g*
Mechanical Vibration Resistance	Mil 883, Method 2007	70	*g*
Max Junction Temperature		130	°C
Storage Temperature		-65 to 150	°C

Table 3. Package Characteristics

Package (mm x mm)	θ-JA (K/W)	θ-JB (K/W)	θ-JC (K/W)	Ψ-JT (K/W) [3]
1.2 x 1.1	206	85	148	14

Note:

3. Refer to SiTime AN23033 application note.

Table 4. Pin Configuration

Pin	Symbol	I/O	Functionality
1	CLK-0	Out	Oscillator Clock Output
2	GND	Power Supply Ground	Connect to Ground
3	NC	NC	No Connect
4	NC	NC	No Connect
5	VDD	Power Supply	Device supply voltage. Under normal operating conditions, VDD does not require external bypass/decoupling capacitor(s). Includes on-chip VDD filtering.
6	NC	NC	No Connect

Typical Performance Plots

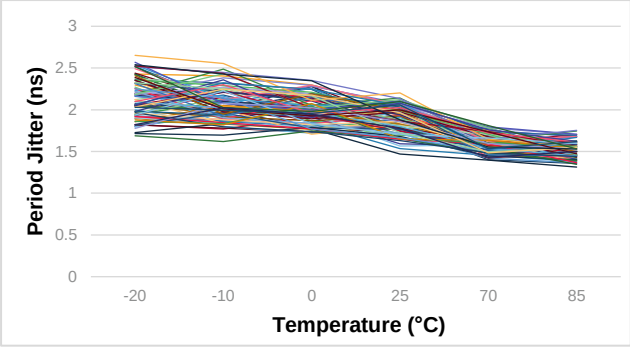


Figure 3. Period Jitter, no supply noise over temperature for VDD = 1.5 V

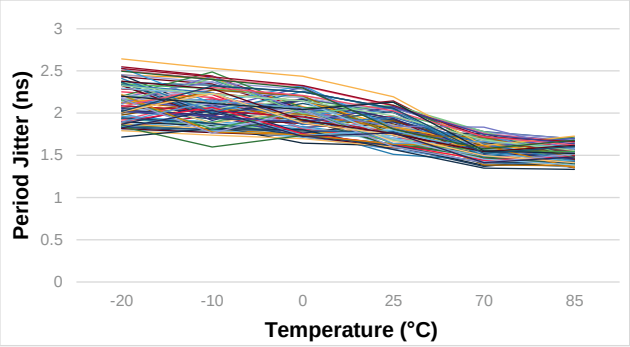


Figure 4. Period Jitter, no supply noise over temperature for VDD = 1.8 V

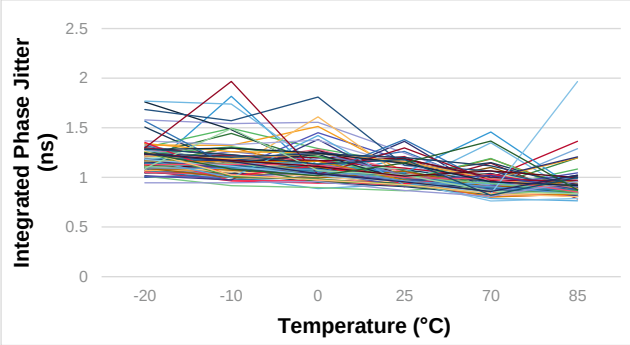


Figure 5. Integrated Phase Jitter, no supply noise over temperature for VDD = 1.5 V

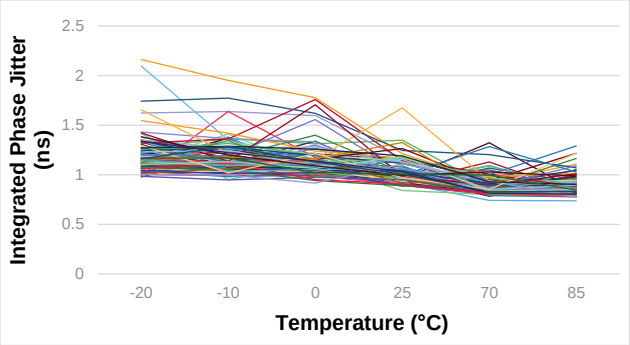


Figure 6. Integrated Phase Jitter, no supply noise over temperature for VDD = 1.8 V

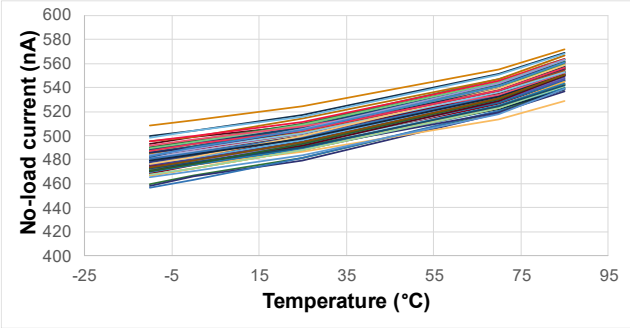


Figure 7. Typical No-load current over temperature for VDD = 1.5 V

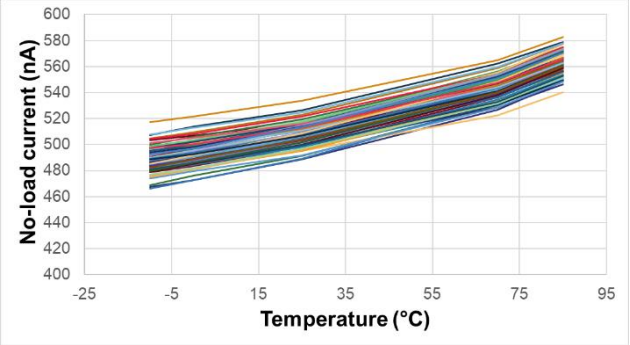


Figure 8. Typical No-load current over temperature for VDD = 1.8 V

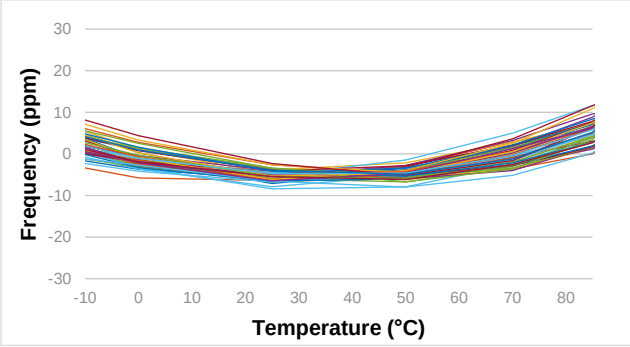
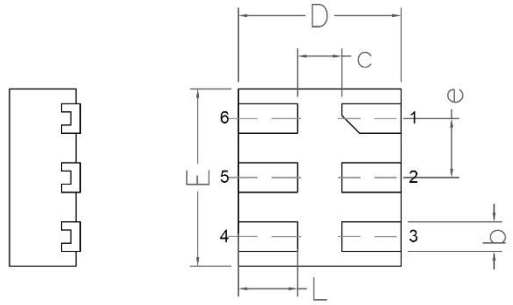
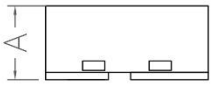


Figure 9. Frequency Vs Temp Stability

Dimensions and Patterns

Package Size – Dimensions (Unit: mm)





POD BOTTOM VIEW

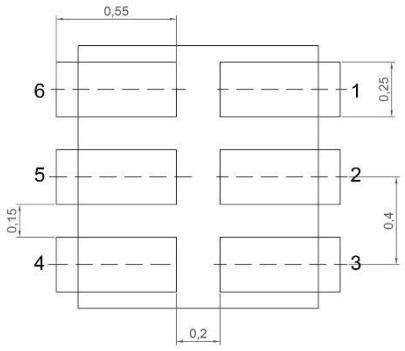
		SYMBOL	MIN	NOM	MAX
TOTAL THICKNESS		A	0.45	0.50	0.55
BODY SIZE	X	D	1.05	1.10	1.15
	Y	E	1.15	1.20	1.25
LEAD WIDTH		b	0.15	0.20	0.25
LEAD LENGTH		L	0.35	0.40	0.45
LEAD PITCH		e	0.35	0.40	0.45
LEAD TO LEAD GAP		c	0.25	0.30	0.35

NOTE:

1. ALL DIMENSION IN MM

PKG INFO		DRAWING NO.
6L QFN 1.20 x 1.10 x 0.50 mm		POD-088-QFN-06-X1211
		REV
DATE	2021/08/11	A00

Recommended Land Pattern (Unit: mm)



Note: All units in mm.

	PKG INFO	SPL DRAWING NO.
	6L QFN 1.20 x 1.10 mm	SPL-088-QFN-06-X01211
DATE		REV
2021/08/23		A00

Layout Guidelines

Sample PCB layout is shown in the following figure. It is strongly recommended that the PCB designer observe the following layout guidelines:

- Do not connect any of the pads directly to a copper polygon or a wide PCB trace. This may cause bad solder joints due to non-uniform heating transfer during the assembly process
- Provide short length (>0.5 mm) and thin width (≤0.25 mm) traces to each pad and then to the respective copper polygon or wide trace
- Keep mirror symmetry of the traces X-Y planes. This will prevent the rotation effect during reflow
- Keep high-current and high-speed traces away from the **oscillator**
  - Route high edge-rate and noisy signals at least 1 mm away from clock-out and pin1 signal traces
  - The use of orthogonal routes is **recommended to avoid signal coupling**

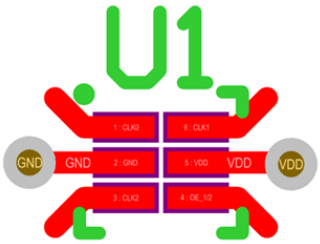


Figure 10. SiT1811 Layout example for board without bypass capacitor

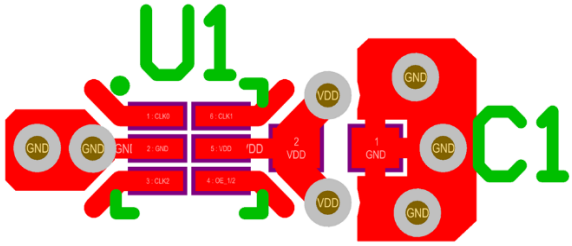


Figure 11. SiT1811 Layout example for board with bypass capacitor

It is recommended to connect VDD and GND pins with polygons or thick wires to corresponding layers of the board. For GND connection it would apply for both device and bypass connections.

- For additional layout recommendations, refer to the Best Design Layout Practices.

Manufacturing Guidelines

The is a precision timing device. Proper PCB solder and cleaning processes must be followed to ensure best performance and long-term reliability.

- For additional manufacturing guidelines and marking/ tape-reel instructions, refer to SiTime Manufacturing Notes.

Revision History

Table 5. Revision History

Version	Release Date	Change Summary
0.1	18-Jun-2021	Advance Datasheet
1.0	22-Feb-2024	Added details to current consumption. Max current increased at 85°C. Add plots for key parameters such as stability over temp, current consumption over temp for 1.5 V and 1.8 V operating voltage, Period Jitter, etc. Removed ordering option for low voltage (1.2 V) and also ±50 ppm Added SiTimeDirect and other links, formatting updates

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